Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	7368	(SIMULAT$4 WITH CIRCUIT) AND DESIGN$4 AND PLAN$5	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/06 07:39
S2	762	S1 and (behav$5 with model)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/04 12:22
S3	248	S2 and (design with specification)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/04 12:23
S4	219	S3 and verif$7	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/04 12:23

S5	217	S4 and input and output	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/04 12:24
S6	11927	((703/13-22) or (716/1-21)).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/02/06 07:41
S7	286	S6 and (design$4 with circuit$2) and board and input and output and verif$7 and behav$5 and (design$4 with specification)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/06 07:43
S8	68	S7 and (floor with plan$5)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/06 08:18
S9	26	S8 and (customer and condition$2 and environment)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/06 11:12

S10	25	S9 and (frequency with operation)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/06 09:08
S11	2685	chip and interconnect$4 and backplane and "25"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/06 08:36
S12	90	chip and interconnect$4 and backplane and S6	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/06 08:36
S13	30	chip and interconnect$4 and backplane and S7	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/06 08:36
S14	35	S8 and (frequency with operation)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/06 11:22

S15	927	(703/14).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/02/06 11:12
S16	246	off with chip with loading	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/06 11:22
S17	11927	((703/13-22) or (716/1-21)).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/02/06 11:22
S18	286	S17 and (design$4 with circuit$2) and board and input and output and verif$7 and behav$5 and (design$4 with specification)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/06 11:22
S19	68	S18 and (floor with plan$5)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/06 11:22

S20	35	S19 and (frequency with operation)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/06 11:22
S21	21	(operating with condition$2) and S20	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/06 11:23